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A CONTACT FOR USE IN AN INTEGRATED CIRCUIT AND A METHOD OF MANUFACTURE THEREFOR

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to a contact and, more specifically, to a contact for use in an integrated circuit, a method of manufacture therefor, and an integrated circuit including the contact.

BACKGROUND OF THE INVENTION

[0002] Devices in the semiconductor industry continue to advance toward higher performance, while maintaining or even lowering the cost of manufacturing. Micro-miniaturization of semiconductor devices has resulted in higher performance, through increases in transistor speed and in the number of devices incorporated in a chip; however, this trend has also increased yield and reliability failures. As contact or via openings decrease in size, the aspect ratio, or the ratio of the depth of the opening to the diameter of the opening, also increases. With a higher aspect ratio, the use of aluminum-based metallization to fill the contact opening, results in electromigration and reliability failures. To alleviate reliability failures, the semiconductor industry has evolved to the use of tungsten, in certain devices, for filling narrow but deep

contact or via openings.

[0003] The switch to tungsten filled contact openings takes advantage of the improved conformal, or step, coverage that results from the use of a plasma enhanced chemical vapor deposition (PECVD) process. In addition, tungsten's high current carrying characteristics reduce the risk of electromigration failure. The conventional method of forming tungsten plugs in vias includes plasma etching of vias or contacts, photoresist striping and cleaning, adhesion layer and barrier metal deposition by physical vapor deposition (PVD) and tungsten deposition by PECVD. Typical adhesion and barrier materials used may consist of a stack of titanium and titanium nitride, respectively. The titanium reduces the contact resistance of the interconnect, and the titanium nitride is a protective layer against titanium attack by a tungsten hexaflouride gas that is used during tungsten deposition. In addition, tungsten adheres to titanium nitride very well, resulting in a mechanically stable tungsten plug.

[0004] Unfortunately, after tungsten plug filling, voids, or so-called tungsten seams, are often observed in the tungsten material. This is particularly the case when the etched via profiles are straight. Such tungsten seams are commonly exposed during subsequent processing, such as during processes designed to remove unwanted tungsten from regions other then the contact opening. Moreover, in certain situations the size of the tungsten seam is

increased due to exposure to the removal process. This often creates a difficult topology for subsequent metallization coverage as well as electrical device degradation, which is especially apparent as leakage in metal-oxide-metal MOM capacitor structures.

[0005] Therefore, processes have been developed, either attempting to create seamless tungsten contact opening fills or repairing the seam or void in the tungsten fill. For example, one attempt involves altering the via etch profile so as to assume a tapered profile, thereby reducing the tungsten seam and allowing better tungsten fill. The tapered via profile helps reduce many of the tungsten seam issues, however, it often leads to increased contact resistance, which is also very undesirable.

[0006] Accordingly, what is needed in the art is a contact structure and method of manufacture therefor that does not experience the tungsten "seam" problems, as experienced in the prior art.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, the present invention provides a contact for use in an integrated circuit, a method of manufacture therefor, and an integrated circuit including the aforementioned contact. The contact, in accordance with the principles of the present invention, may include a via located in a substrate, and a contact plug located in the via, wherein the contact plug has a first portion having a notch removed therefrom and a second portion filling the notch.

[0008] As previously mentioned, the present invention also provides a method form manufacturing the contact disclosed above. Among other steps, the method includes forming a via in a substrate, and placing a contact plug in the via, wherein the contact plug has a first portion having a notch removed therefrom and a second portion filling the notch.

[0009] Additionally, the present invention provides an integrated circuit including the aforementioned contact. The integrated circuit, among other elements, includes: (1) transistors located over a substrate, (2) an interlevel dielectric layer located over the transistors, the interlevel dielectric layer having a contact for contacting the transistors located therein, the contact including a via located in the interlevel dielectric

layer and a contact plug located in the via, wherein the contact plug has a first portion having a notch removed therefrom and a second portion filling the notch.

[0010] The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The invention is best understood from the following detailed description when read with the accompanying FIGUREs. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0012] FIGURE 1 illustrates a cross-sectional view of one embodiment of a portion of an integrated circuit constructed according to the principles of the present invention;

[0013] FIGURE 2 illustrates a cross-sectional view of a partially completed integrated circuit at an initial stage of manufacture;

[0014] FIGURE 3 illustrates a cross-sectional view of the partially completed integrated circuit illustrated in FIGURE 2 after depositing a layer of conductive material, such as tungsten, within the trench, and thereafter polishing it back, resulting in an initial contact plug;

[0015] FIGURE 4 illustrates a cross-sectional view of the partially completed integrated circuit illustrated in FIGURE 3 after etching a notch from the initial contact plug;

[0016] FIGURE 5 illustrates a cross-sectional view of the partially completed integrated circuit illustrated in FIGURE 4 after an optional adhesion layer has been formed over the substrate and within the notch created in the initial contact plug;

[0017] FIGURE 6 illustrates a cross-sectional view of the partially completed integrated circuit illustrated in FIGURE 5 after forming a second conductive material over the adhesion layer and filling the notch in the initial contact plug; and

[0018] FIGURE 7 illustrates a cross-sectional view of an integrated circuit (IC) incorporating contacts constructed according to the principles of the present invention.

DETAILED DESCRIPTION

[0019] Referring initially to FIGURE 1, illustrated is a cross-sectional view of one embodiment of a portion of an integrated circuit 100 constructed according to the principles of the present invention. In the embodiment illustrated in FIGURE 1, the integrated circuit 100 includes a dielectric layer 110 having a conductive feature 120 located therein. The dielectric layer 110 might be an interlevel dielectric layer and the conductive feature 120 might be a runner located within the dielectric layer 110 for connecting various features in the integrated circuit 100. Other dielectric layers and conductive features are within the scope of the present invention.

[0020] Located over the dielectric layer 110 and the conductive feature 120 is a substrate 130. The substrate 130, similar to the dielectric layer 110, may comprise an interlevel dielectric layer. However, the substrate 130 may comprise other layers and stay within the scope of the present invention. Located within the substrate 130 and over the conductive féature 120 is a contact 140. The contact 140 is configured to provide electrical contact to the conductive feature 120.

[0021] In the embodiment illustrated in FIGURE 1, the contact 140 includes a via 150 located within the substrate 130. Located within the via 150 is a contact plug 160. The contact plug 160

constructed in accordance with the principles of the present invention includes a first portion 170, wherein the first portion 170 has a notch removed therefrom. This notch is present as a result of the first portion originally including a seam, and it subsequently being etched away, thus resulting in the notch shown.

[0022] As shown in FIGURE 1, the contact plug 160 further includes a second portion 180. FIGURE 1 illustrates that the second portion 180 may be used to completely fill the notch of the first portion 170. Notice how the profile of the notch of the first portion 170 is dissimilar to the profile of the trench 150. That is, the notch of the first portion 170, and thus the second portion 180 that fills the notch, is not conformal with the sidewalls of the trench as might be seen in traditional devices. This non-conformal second portion 180 is a result of the unique method for manufacturing the contact 140.

[0023] Optionally located between the first and second portions 170, 180, is an adhesion layer 190. The adhesion layer 190, which may comprise a titanium/titanium nitride adhesion layer or other similar materials, may be used to provide the requisite adhesion between the first and second portions 170, 180. Even though the first and second portions 170, 180, may comprise the same material (e.g., tungsten), the adhesion layer 190 is desired in certain applications.

[0024] What results is a contact 140 being substantially free of

a seam or void. As the contact 140 is substantially free of a seam or void, as compared to many of the prior art structures, especially those using tungsten as the conductive material, it does not experience the topology and electrical device degradation issues experienced by the prior art structures. Additionally, the contact 140 is easy to manufacture and can be smoothly incorporated into the already existing process flow.

[0025] Turning now to FIGUREs 2-6, illustrated are cross-sectional views of detailed manufacturing steps instructing how one might, in an advantageous embodiment, manufacture an integrated circuit similar to the integrated circuit 100 depicted in FIGURE 1. FIGURE 2 illustrates a cross-sectional view of a partially completed integrated circuit 200 at an initial stage of manufacture. The partially completed integrated circuit 200 includes a dielectric layer 210 having a conductive feature 220 located therein. As previously recited, the dielectric layer 210 could be an interlevel dielectric layer or another similar layer, as well as the conductive feature 220 could be a trace, interconnect, etc.

[0026] Located over the dielectric layer 210 and the conductive feature 220 is a substrate 230. More often than not the substrate 230 is an interlevel dielectric layer. It should be noted, however, that the substrate 230 could be any layer located within an integrated circuit, and particularly any insulative layer.

[0027] Conventionally formed within the substrate 230 in the embodiment shown and discussed with respect to FIGURE 2 is a trench 240. The trench 240 is a standard trench that might be used in an integrated circuit to connect various layers therein. For example, a trench having an opening width ranging from about 100 nm to about 300 nm, and a depth ranging from about 400 nm to about 1200 nm, or other dimensions, could be used.

[0028] While not shown, the trench could be formed by patterning the blanket substrate 230 using photoresist and/or a hardmask layer. As those skilled in the art understand the various number of ways the trench 240 may be formed, no further detail is required.

[0029] Turning now to FIGURE 3, illustrated is a cross-sectional view of the partially completed integrated circuit 200 illustrated in FIGURE 2 after depositing a layer of conductive material, such as tungsten, within the trench 240, and thereafter polishing it back, resulting in an initial contact plug 310. Notice how the initial contact plug 310 of FIGURE 3 has a seam or void 320 located therein. As is often the case, this seam or void 320 is a result of the type of conductive material used to fill the trench 240. Tungsten, for example, is known for forming such seams or voids 320. Unfortunately, these seams or voids 320 are highly undesirable.

[0030] Turning now to FIGURE 4, illustrated is a cross-sectional

view of the partially completed integrated circuit 200 illustrated in FIGURE 3 after etching a notch 410 from the initial contact plug 310. The notch 410, which attempts to remove at least a portion of the seam or void 320, or alternatively an entire portion of the seam or void 320, typically has a profile that is dissimilar to the profile of the trench 240. For example, a V-shaped notch positioned only where the previous seam of void 320 was located, may be used in an exemplary embodiment. Other notch shapes, however, could also be used.

[0031] The notch 410 optimally has an opening width that ranges from about 50 nm to about 150 nm. Similarly, the notch 410 may have a depth ranging from about 20 nm to about 600 nm. This depth may vary as long as it encompasses a large portion of the seam or void 320, or optimally the entire portion of the seam or void 320.

[0032] Those skilled in the art understand the various techniques that could be used to create the notch 410. In one embodiment of the invention a protective mask is used to isolate the initial contact plug 310, while a chemical etch is subjected thereto. For example a reactive ion etch (RIE) or other similar etch could be used.

[0033] Turning now to FIGURE 5, illustrated is a cross-sectional view of the partially completed integrated circuit 200 illustrated in FIGURE 4 after an optional adhesion layer 510 has been formed over the substrate 230 and within the notch 410 created in the

initial contact plug 310. The adhesion layer 510 in one embodiment comprises a titanium/titanium nitride adhesion layer having a thickness ranging from about 5 nm to about 15 nm. Other materials, as well as other thicknesses, could also be used. As the adhesion layer 510 is a conventional adhesion layer, it may be formed using a number of different conventional processes. For example, a conventional chemical vapor deposition (CVD), physical vapor deposition (PVD) or other similar deposition process could be used.

[0034] Turning now to FIGURE 6, illustrated is a cross-sectional view of the partially completed integrated circuit 200 illustrated in FIGURE 5 after forming a second conductive material 610 over the adhesion layer 510 and filling the notch 410 in the initial contact plug 310. The second conductive material 610, in an exemplary embodiment, comprises a similar material as the initial contact plug 310. For example, tungsten could be a good choice as both the initial contact plug 310 and the second conductive material 610. Other materials are, however, within the scope of the present invention, including different materials for the different portions.

[0035] The second conductive material 610 may be formed using similar processes as the initial contact plug 310. Additionally, the second conductive material 610 may be formed having a thickness ranging from about 50 nm to about 150 nm, or other thicknesses outside that range. Nonetheless, it is important that the second

conductive material 610 substantially fill the notch 410.

[0036] After completing the partially completed integrated circuit 200 illustrated in FIGURE 6, the second conductive material 610 may be polished. What results is a completed integrated circuit, including a contact plug located within a via, wherein the contact plug has a first portion with a notch removed therefrom, and a second portion filling the notch. Such a device could be similar to the integrated circuit 100 illustrated in FIGURE 1.

[0037] Referring finally to FIGURE 7, illustrated is a cross-sectional view of an integrated circuit (IC) 700 incorporating contacts constructed according to the principles of the present invention. The IC 700 may include devices, such as transistors used to form CMOS devices, BiCMOS devices, Bipolar devices, or other types of devices. The IC 700 may further include passive devices, such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of devices and their manufacture.

[0038] In the particular embodiment illustrated in FIGURE 7, the IC 700 includes semiconductor devices 710 located between isolation structures 720. The IC 700 of FIGURE 7 further includes dielectric layers 730 located over the semiconductor devices 710. Additionally, contacts 740 constructed in accordance with the principles of the present invention are located within the

dielectric layers 730 to interconnect various devices, thus, forming the operational IC 700.

[0039] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.